IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A leadframe comprising:

an outer frame with a plurality of sides surrounding a region of the leadframe on which a semiconductor chip is to be mounted;

a die pad on which the semiconductor chip is to be mounted; [[and]]

a plurality of leads each having land portions and connections, the land portions each having an upper surface serving as a bonding pad to be connected with a metal wiring and a lowermost part serving as an external terminal, the connections each being devoid of its lower part so as to be thinner than the land portion and being provided between the outer frame and the land portions, between the land portions associated with each other in each lead, and between the land portions and the die pad; and [[,]]

at least one land formed in a corner region of the outer frame and connected to the outer frame through a connection, said at least one land having a larger area than the land portions, and

wherein the die pad and the outer frame are connected to each other via the land portions and the connections.

2. (Original) The leadframe according to claim 1, wherein the lowermost parts of the land portions are substantially identical in shape in plan view and are arranged in a lattice pattern.

3. (Original) The leadframe according to claim 1, wherein three or more rows of the lowermost parts of the land portions are arranged along each side of the outer frame.

4. (Original) The leadframe according to claim 1, wherein the plurality of leads include a lead that is connected to one side of the outer frame and is connected to the other lead that is connected to the other side of the outer frame adjacent to the one side thereof.

5. (Currently amended) [[A]] The leadframe [[comprising:]] according to claim 1, wherein ~~an outer frame with a plurality of sides surrounding a region of the leadframe on which a semiconductor chip is to be mounted; a~~ the die pad [[having]] has a thin portion that is provided along the peripheral section of the main body of the die pad and [[that]] is devoid of its lower part, and a plurality of heat dissipating terminals each protruded downward from the lower surface of the thin portion~~; and~~

~~a plurality of leads each having land portions and connections, the land portions each having an upper surface serving as a bonding pad to be connected with a metal wiring and a lowermost part serving as an external terminal, the connections each being devoid of its lower part so as to be thinner than the land portion and being provided between the outer frame and the land portions, between the land portions associated with each other in each lead, and between the land portions and the heat dissipating terminals~~.

6. (Original) The leadframe according to claim 5, wherein the land portions and the heat dissipating terminals are substantially identical in shape in plan view and are arranged in a lattice pattern.

7. (Original) The leadframe according to claim 5, wherein the land portions and the heat dissipating terminals are arranged at substantially fixed pitch intervals in at least one direction.

8. (Original) The leadframe according to claim 5, wherein three or more rows of the land portions are arranged along each side of the outer frame.

9. (Original) The leadframe according to claim 5, wherein there exists no member that functions as a suspension lead during plastic encapsulation.

10-23. (Cancelled)

24. (New) A plastic-encapsulated semiconductor device comprising:

a die pad;

a semiconductor chip mounted on the die pad;

land portions each detached from the die pad and each having an upper surface serving as a bonding pad to be connected with a metal wiring and a lowermost part serving as an external terminal;

a plurality of connecting members through which portions of the semiconductor chip are connected to the bonding pads;

at least one land formed in a corner region having a larger area than the land portions; and

a plastic encapsulant for encapsulating the semiconductor chip, the connecting members, the land portions, the land and the die pad, with the lowermost parts of the land portions and the land and at least a part of the bottom surface of the die pad exposed,

the semiconductor device is provided with no member that extends from the die pad and that has its end exposed at a surface of the plastic encapsulant.

25. (New) The semiconductor device according to claim 24, wherein the external terminals are substantially identical in shape in plan view and are arranged in a lattice pattern at the bottom surface of the plastic encapsulant.

26. (New) The semiconductor device according to claim 24, wherein three or more rows of the external terminals are arranged at the bottom surface of the plastic encapsulant along the peripheral region thereof.

27. (New) The semiconductor device according to claim 24, wherein the die pad has a thin portion that is provided along the peripheral section of the main body of the die pad and that is devoid of its lower part, and a plurality of heat dissipating terminals each protruded downward from the lower surface of the thin portion.